Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A bi-directional communication link having plural channels, each of said channels comprising:

a master connected at a near end of the channel and a slave connected at an opposite end of the channel;

said master comprising:

(a) a transmitter coupled to the channel and having a master Tx clock signal; and

(b) a receiver coupled to the channel and comprising:

(i) an analog-to-digital converter that periodically samples at a sampling time Ts;

(ii) a clock recovery circuit that generates a master Rx clock from a clock signal embedded in a signal received from the channel; and

(iii) a metric processor connected to an output of said analog-to-digital converter that produces a metric signal ~~indicative of resolution~~ reflective of amplitude differences between the received signal and allowed amplitude levels of the received signal; and

said slave comprising:

(a) a receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from the signal received from the master;

(b) a transmitter coupled to the channel and having a Slave Tx clock signal, whereby said master Rx clock signal is frequency locked to said Slave Tx clock signal; and

(c) a first controllable delay element for generating said Slave Tx clock signal from said Slave Rx clock signal; and

said communication link further comprising a decision processor responsive to said metric processor for changing a delay value of said controllable delay element so as to maximize the metric signal.

Claims 2-3 (canceled)

Claim 4 (original): The apparatus of claim 1 further comprising a second controllable delay between said Master Rx clock signal and said analog-to-digital converter and responsive to said decision processor, whereby said decision processor delays the Slave Tx clock signal and the sample time Ts independently to maximize the metric signal.

Claim 5 (currently amended): A bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, said bi-directional communication link comprising:

a metric processor for each master that produces a metric signal ~~indicative of resolution~~ reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal; and

a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to maximize the metric signal.

Claims 6-7 (canceled)

Claim 8 (currently amended): A bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, said bi-directional communication link comprising:

a metric processor for each master that produces a metric signal ~~indicative of resolution~~ reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal; and

a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal.

Claims 9-10 (canceled)

Claim 11 (currently amended): A bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx

clock frequency-locked to the Slave Rx clock, wherein each master receives a periodic noise burst comprising cross-talk from masters of adjacent channels and echoes of itself, ~~said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication,~~ said bi-directional communication link comprising:

a metric processor for each master that produces a metric signal ~~indicative of the resolution~~ reflective of amplitude differences between of the signal received by the master from the corresponding slave and allowed amplitude levels of the received signal; and

a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal.

Claims 12-13 (canceled)

Claim 14 (currently amended): A bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk from masters of adjacent channels and echoes of itself, ~~said noise capable of reducing the resolution of a signal received by the master from the slave~~

~~over the corresponding communication,~~ said bi-directional communication link comprising:

a metric processor for each master that produces a metric signal ~~indicative of the resolution~~ reflective of amplitude differences between the signal received by the master from the corresponding slave and allowed amplitude levels of the received signal; and

a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal.

Claims 15-18 (canceled)

Claim 19 (currently amended): The apparatus of claim ~~16~~ 14 wherein said metric processor comprises a processor for computing the proportion of samples of the signal received by ~~the~~ said each master falling within allowed amplitude levels relative to those that fall outside of said allowed amplitude levels.

Claim 20 (currently amended): In a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk from masters of adjacent

channels and echoes of itself, ~~said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication,~~ a method of reducing the effects of the cross-talk and echo noise burst on the signal received by each master, comprising:

for said each master, producing a metric signal ~~indicative of the resolution~~ reflective of amplitude differences between the signal received by the master from the corresponding slave and allowed amplitude levels of the received signal; and

in response to said metric signal, shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal.

Claims 21-22 (canceled)

Claim 23 (currently amended): The method of claim 20 wherein the shifting ~~of said sample time Ts is carried out by~~ step comprises the step of changing a delay between said Slave Rx clock and said Slave Tx clock.

Claim 24 (canceled)

Claim 25 (currently amended): The method of claim ~~22~~ 20 wherein the producing ~~of the metric signal~~ step comprises the step of computing ~~the~~ a proportion of samples of the signal received by ~~the~~ said each master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels.

Claim 26 (canceled)

Claim 27 (new): The apparatus of claim 1 wherein said metric processor comprises a processor for computing the proportion of samples of the signal received by the master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels.

Claim 28 (new): The apparatus of claim 5 wherein said metric processor comprises a processor for computing the proportion of samples of the signal received by said each master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels.

Claim 29 (new): The apparatus of claim 8 wherein said metric processor comprises a processor for computing the proportion of samples of the signal received by said each master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels.

Claim 30 (new): The apparatus of claim 11 wherein said metric processor comprises a processor for computing the proportion of samples of the signal received by said each master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels.